IN THE SPECIFICATION:

Please rewrite the paragraph at page 12, line 3 to page 13, line 2, so that it reads as follows:

The reason for including the cascode transistors is to increase the output impedance of the current mirrors 322 and 324. Thus the variation of output current I_{CP} is less dependent on the output voltage and the voltage range over which the output current I_{CP} is generated can be improved. It should be noted that the switching transistors M3A and M3X are coupled to respective transistors M37 and M38 in cascode rather than directly to the output node 325 so that switching noise from operation of the switches is isolated from the output node 325. Furthermore, the effective gate-source voltage of each output mirror transistor is well matched in the arrangement of the charge pump 320 by the principles of the invention. This leads to a more accurate matching in the mirror current. By analysis and simulation, it is found that the charge pump of the invention causes less charge accumulation on the parasitic capacitance than the one proposed in U.S. Pat. No. 6,160,432, which effectively results in a reduction of the turn-on time. FIG. 4 demonstrates the simulation result comparing the invention and the prior art. In the simulation, the operating speed is assumed to be 125 MHz. The output current of the invention is plotted with the solid line while the output current of U.S. Pat. No. 6,160,432 is plotted with the dash line. From FIG. 4, it can be seen that the ~~turn-on time~~ magnitude of the current swing of the invention is ~~half as long as the turn-on time~~ greater than that of the prior art approximately. Compared to the prior art, therefore, the present invention provides a charge pump having high switching speed, low switching noise and better current matching.

Please rewrite the paragraph at page 14, line 22 to page 15, line 20, so that it reads as follows:

In a similar fashion, the p-channel wide-swing cascade current mirror 522 is made up of transistors M51, M53, M55 and M57. The switching transistor M5A is interposed between the output mirror transistor M53 and the output cascode transistor M57. The switching transistor M5A has its source coupled to the drain of the output mirror transistor M53, its drain coupled to the source of the output cascode transistor M57, and accepts a control signal UP at its gate. Correspondingly, the transistor M5B is interposed between the input mirror transistor M51 and the input cascode transistor M55. The transistor M5B has its source coupled to the drain of the input mirror transistor M51 and its drain coupled to the source of the input cascode transistor M55. The gate of the transistor M5B is coupled to the low-potential voltage supply, namely ground, in order to bring about conduction in the transistor M5B continuously. The input mirror transistor M51 has its gate coupled to the gate of the output mirror transistor M53. The sources of transistors M51 and M53 are connected together to V_{DD}. The output cascode transistor M57 has its drain coupled to the drain of the output cascode transistor M58 at the output node 525. The input cascode transistor M55 has its drain coupled to the gate of the input mirror transistor M51. The reference current source 526 is connected to the drain of the input cascode transistor M55. The gates of transistors M55 and M57 are connected together. The transistors M55 and M57 both have gate voltages established by a bias voltage V_{B2}. The bias voltage V_{B2} should be sufficient to turn on the cascode transistors ~~M35 and M37~~ M55 and M57.